Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAVI KUMAR ARIMILLI, LEO JAMES CLARK, JOHN STEVE DODSON, GUY LYNN GUTHRIE, and JERRY DON LEWIS

Appeal No. 2003-0376
Application 09/364,281

ON BRIEF

Before KRASS, JERRY SMITH, and LEVY, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-3, 5-9, 11-15, 17 and 18, which constitute all the claims remaining in the application.

The disclosed invention pertains to a data processing system having redundant hardware partitions that provide dynamic repair capability. If an error is detected in a particular hardware partition, the data stream assigned to that hardware partition is reassigned to another of the plurality of hardware partitions. The data streams are assigned to the hardware partitions using a hashing circuit and a hashing selection circuit. When an error is detected in a particular hardware partition, the hashing selection circuit reassigns a data stream by changing the hash implemented by the hashing circuit.

Representative claim 1 is reproduced as follows:

1. A processor, comprising

execution resources;

data storage; and

an instruction sequencing unit, coupled to said execution resources and said data storage, that supplies instructions within said data storage to said execution resources;

wherein of said execution resources, said data storage, and said instruction sequencing unit, at least said execution resources are implemented with a plurality of hardware partitions of like function for processing a respective one of a plurality of data streams, and wherein said instruction sequencing unit includes a hashing circuit that assigns said plurality of data streams to said plurality of hardware partitions based upon an address hash of addresses associated with instructions within said plurality of data streams, said hash being selected by a hash selection circuit within said processor, and wherein if an

error is detected in a particular hardware partition among said plurality of hardware partitions that is assigned a particular data stream among said plurality of data streams to process, said hashing selection circuit reassigns said particular data stream to at least one other of said plurality of hardware partitions by changing the address hash implemented by the hashing circuit.

The examiner relies on the following references:

Walter et al. (Walter)	4,933,940	June 12, 1990
Edwards et al. (Edwards)	5,649,090	July 15, 1997
Eberhard et al. (Eberhard)	5,713,001	Jan. 27, 1998

Claims 1-3, 5-9, 11-15, 17 and 18 stand rejected under 35 U.S.C. § 103(a). As evidence of obviousness the examiner offers Walter in view of Eberhard with respect to claims 1, 3, 5-7, 9, 11-13, 15, 17 and 18, and Edwards is added to this combination for claims 2, 8 and 14.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the examiner and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's

rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in the claims on appeal. Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir.), cert. denied, 488 U.S. 825 (1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.,

776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985), cert. denied, 475 U.S. 1017 (1986); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See Id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered and are deemed to be waived by appellants [see 37 CFR § 1.192(a)].

We consider first the rejection of claims 1, 3, 5-7, 9, 11-13, 15, 17 and 18 based on Walter and Eberhard. These claims stand or fall together as a single group [brief, page 5], and we will consider independent claim 1 as the representative claim for

this group. With respect to representative claim 1, the examiner essentially finds that the reconfiguration mode disclosed by Walter teaches the claimed invention except that Walter does not disclose a hashing circuit that assigns an address hash of addresses associated with instructions within a plurality of data streams. The examiner cites Eberhard as teaching the generation of hashed virtual addresses from address operands. The examiner finds that it would have been obvious to the artisan to include the hashing circuit of Eberhard in the reconfiguration mode of Walter because assigning an active task set a numerical value so that it can be associated with a particular node performs the same function as allocating to each node an active task set through a reconfiguration algorithm [Final Rejection mailed April 11, 2002, incorporated into answer at page 3].

Appellants argue that neither applied reference discloses the claimed hashing circuit or the hashing selection circuit. Appellants argue that even if Eberhard were to be combined with Walter, the combination would still not disclose the hashing circuit as specifically set forth in claim 1. Appellants also argue that an address is not employed to allocate tasks to nodes in Walter. Appellants note that Eberhard relates only to an

improved cache system and not to the assignment of data streams to hardware partitions [brief, pages 5-9].

The examiner responds that he defines hashing as taking an address and mapping it to a numerical value by a transformation known as a hashing function. The examiner asserts that Eberhard was used to show that it was "well known in the art to hash addresses" and that Walter teaches assigning tasks to nodes. The examiner asserts that hashing is used to assign tasks to the nodes in Walter. The examiner also asserts that a hashing circuit included in the processor would be "inherent" in the combined system. The examiner responds that hashing is used to assign tasks to the nodes because of the use of addresses in Walter. The examiner also asserts that a hash selection circuit is "inherent" to a hashing circuit. The examiner notes that it is "inherent" to the system of Walter to use addresses to assign active tasks and that these addresses are hashed [answer, pages 3-9].

Appellants respond that the combination of Walter and Eberhard fails to teach a hashing circuit that assigns said plurality of data streams to said plurality of hardware partitions based upon an address hash of addresses associated with instructions within said plurality of data streams as

claimed. Appellants also respond that the combined references fail to teach the assignment of tasks to nodes based upon hashed addresses or a hashing circuit that performs such assignment. Appellants argue that a hashing selection circuit is not inherently present in the applied prior art [reply brief].

We will not sustain the examiner's rejection of claims 1, 3, 5-7, 9, 11-13, 15, 17 and 18 for essentially the reasons argued by appellants in the briefs. In our view, the examiner has done nothing more than find a first reference that teaches hardware reconfiguration with absolutely no suggestion of address hashing with a second reference that broadly teaches hashing addresses for a cache memory with absolutely no other indicated uses. The examiner has then attempted to cobble a rejection by picking and choosing selected parts of these references and by dismissing specific features of the claimed invention as being well known and inherent. The examiner's first major mistake is to assume that if addressing is present, then hashing must also necessarily be present. There is no requirement that hardware addressing make use of a hashing algorithm. The second major mistake made by the examiner is to assume that the general hashing scheme used by Eberhard for cache accessing automatically suggests using a hash addressing scheme for the node accessing

system of Walter. We can find no valid basis for motivating the artisan to apply the cache hash addressing teachings of Eberhard to the hardware system of Walter.

The examiner's rejection also fails because it substantially relies on inherency to support the examiner's findings. As argued by appellants, an examiner cannot rely on inherent properties of a reference unless the inherent properties relied on are necessarily present in the applied prior art. The examiner's findings of inherency on this record are based on nothing more than the examiner's mere opinion. We agree with appellants that the claimed hash circuit and hash selection circuit, as specifically recited in the claims on appeal, are not inherent in the teachings of Eberhard and Walter whether taken alone or in combination.

We now consider the rejection of claims 2, 8 and 14 based on Eberhard, Walter and Edwards. Since Edwards does not overcome the deficiencies in the combination of Eberhard and Walter discussed above, we also do not sustain the examiner's rejection of these claims.

In summary, we have not sustained either of the examiner's rejections of the claims on appeal. Therefore, the decision of the examiner rejecting claims 1-3, 5-9, 11-15, 17 and 18 is reversed.

REVERSED

ERROL A. KRASS Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
STUART S. LEVY Administrative Patent Judge	)	

JS/dym

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